UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/670,231	09/28/2000	John S. Sadowsky	INTL-0328-US (P8031)	7225

7590 04/15/2004

Timothy N Trop
Trop Pruner & Hu PC
Suite 100
8554 Katy Freeway
Houston, TX 77024

EXAMINER	
CHAUDRY, MUJTABA M	
ART UNIT	**PAPER NUMBER**
2133	10

DATE MAILED: 04/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/670,231	SADOWSKY, JOHN S.	
	Examiner	Art Unit	
	Mujtaba K Chaudry	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12 and 21-26* is/are pending in the application.

4a) Of the above claim(s) *13-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 21* is/are rejected.

7)☒ Claim(s) *7-12 and 22-26* is/are objected to.

8)☒ Claim(s) *13-20* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 September 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

In view of the Appeal Brief filed on January 26, 2004 and interview with Applicant's attorney, PROSECUTION IS HEREBY REOPENED. A new ground of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) File a reply under 37 CFR 1.111 (since this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) Request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

Election/Restrictions

Restriction to one of the following inventions is required under 35 USC 121:

I. Claims 1-12 and 21-26, drawn to system having a signal processor comprising a bus connected to a memory and a butterfly coprocessor, classified in class 714, subclass 31.

II. Claims 13-20, drawn to identifying a stage of trellis diagram and calculating branch metrics for each node, classified in class 714, subclass 796.

The inventions are distinct, each from the other because of the following reasons:

Inventions Group I, system having a signal processor comprising a bus connected to a memory and a butterfly coprocessor and Group II, identifying a stage of trellis diagram and calculating branch metrics for each node related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed because the functionality of system in Group I does not require to calculate branch metrics for each node in a trellis diagram. The subcombination has separate utility such as in a single networked environment.

During a telephone conversation with Attorney, Mark J. Rozman (512-418-9944)on Wednesday, March 31, 2004 a provisional election was made without traverse to prosecute the invention of Group I, which include claims 1-12 and 21-26 and are classified in class 714/730. Affirmation of this election must be made by applicant in replying to this Office action. Claims of Group II, which include claims 13-20, classified in class 714/796, are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention. Applicant is reminded that non-elected claims need to be cancelled in subsequent office action.

Response to Amendment

Applicant's arguments with respect to previously submitted claims 1-26 filed January 26, 2004 have been fully considered and in view of restriction requirements hereinabove, claims 1-12 and

21-26 have been elected without traverse and are examined. Applicant is reminded non-elected claims 13-20 must be cancelled in subsequent response.

Allowable Subject Matter

Claim 22 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Furthermore, dependent claims 7-12 and 23-26 would be allowable as well if the limitations of claims 22 are incorporated within claims 1 and 21.

Reasons for indicating allowable subject matter:

Dependent Claim 22 teaches the system comprising a digital signal processor having a bus connected to a memory, a data address generator and a arithmetic unit and a butterfly coprocessor, wherein the digital signal processor has a software program which causes the system to identify a stage of a trellis diagram with the number of nodes in each stage with the number of branches extending form each node. The prior art of record, namely Murakami et al. (herein after: Murakami) teaches a digital signal processor of a simple circuit configuration capable of implementing arithmetic processes and interruption processes efficiently in a reduced number of steps at a high processing speed. The digital signal processor comprises instruction execution pipeline stages including a stage in which data is read from a data memory and the data is applied to an arithmetic unit; an arithmetic unit for the execution stage, including a barrel shifter, a multiplier and an arithmetic and logic unit, a normalizing barrel shifter, a round-off/accumulation adder, internal data memories and a DMA transfer bus for a write/accumulation stage, an address generating unit capable of parallel and two-dimensional generation of two

inputs one output data memory addresses and a DMA control unit for controlling the two-dimensional data transfer through a DMA bus between the internal data memories and an external data memory for an instruction execution stage. In particular, Murakami teaches (Figure 38) system comprising a digital signal processor (404) coupled to an external memory (413) and a host processor (403), which is analogous to the butterfly coprocessor of the present application. Furthermore, Murakami teaches a data address generator and a arithmetic unit to be incorporated within the program counter (407). However, Murakami fails to teach a digital signal processor having a bus connected to a memory, a data address generator and a arithmetic unit and a butterfly coprocessor, wherein the **digital signal processor has a software program which causes the system to identify a stage of a trellis diagram with the number of nodes in each stage with the number of branches extending form each node**. [Emphasis added] Therefore, the prior art does not fairly teach nor suggest to teach the limitations as suggested by those of claim 22.

Claim Objections

Claims 1 and 21 are objected to because of the following informalities:

- The preambles of the claims do not suggest what the system is utilized for. Applicants are strongly recommended to insert language that introduces the use of the system in the preambles of the claims.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 21 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. For example, it is not clear if the components, bus, address generator and arithmetic unit are comprised onto the digital signal processor which is comprised onto the system or if the said components are just on the system alongside with said digital signal processor. Applicants are requested to modify claim language to clarify ambiguity.

Claims 22-26 inherently depend from claim 21 and inherently include limitations therein and therefore are rejected as well.

Claim Rejections - 35 USC § 103

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-6 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murakami et al. (USPN 5045993).

As per claims 1 and 21, Murakami et al. (herein after: Murakami) substantially teaches (title and abstract) a digital signal processor of a simple circuit configuration capable of implementing arithmetic processes and interruption processes efficiently in a reduced number of steps at a high processing speed. The digital signal processor comprises instruction execution pipeline stages including a stage in which data is read from a data memory and the data is applied to an arithmetic unit; an arithmetic unit for the execution stage, including a barrel shifter, a multiplier and an arithmetic and logic unit, a normalizing barrel shifter, a round-off/accumulation adder, internal data memories and a DMA transfer bus for a write/accumulation stage, an address generating unit capable of parallel and two-dimensional generation of two inputs one output data memory addresses and a DMA control unit for controlling the two-dimensional data transfer through a DMA bus between the internal data memories and an external data memory for an instruction execution stage. In particular, Murakami teaches (Figure 38) system comprising a digital signal processor (404) coupled to an external memory (413) and a host processor (403), which is analogous to the butterfly coprocessor of the present application. Furthermore, Murakami teaches a data address generator and a arithmetic unit to be incorporated within the program counter (407).

Murakami does not explicitly teach the coprocessor or the host processor (403) to be a butterfly coprocessor as stated in the present application.

However, the present application defines the coprocessor (specification, page 17, lines 24-28) the butterfly coprocessor to perform add-compare-select functions. In the reference, Murakami teaches, referring to Figure 38, a host processor 403, a signal processor 404, a hold request signal 405 requesting the temporary stop of instruction execution of the signal processor

404, a hold authorizing signal 406 for informing an external unit of the temporary stop of the signal processor 404, a program counter (PC) 407, an instruction memory control unit 408, a reloadable writable instruction memory 409, an instruction address 410, a switching circuit 411, a selection signal 412, an external instruction memory 413, instruction words 414 and 415, a comparing circuit 416, a result 417 of decision, and write end signal 418. The signal processor 404 has an arithmetic unit the same as that of the conventional signal processor, and hence the arithmetic unit is not shown in FIG. 38. In Figure 39, Murakami teaches a flow chart of in explaining the operation of the signal processor. When the content of a process to be executed by the signal processor 404 needs to be changed, the host processor 403 (analogous to butterfly coprocessor) gives the signal processor 404 the hold request signal 405 requesting the temporary stop of instruction word execution. Upon the end of an instruction presently being executed after the reception of the hold request signal 405, the signal processor 404 provides the hold authorizing signal 406 to stop updating the PC 407 and to interrupt the execution of the instruction word temporarily. Then, the instruction memory control unit 408 provides the instruction address 410 specifying an address to be reloaded in the writable instruction memory 409, and the selection signal 412 to control the switching circuit 411 so that the instruction address 410 is selected. At the same time, the instruction address 410 is given also to the external instruction memory 413. Then, the external instruction memory 413 provides an instruction word 414, which is written in the writable instruction memory 409. The instruction word 414 is written in the writable instruction memory 409 is read from the writable instruction memory 409. The instruction word 415 read from the rewritable instruction memory 409 and the instruction word 414 written in the same are compared by the comparison circuit 416 to decide

whether or not the instruction words 414 and 415 coincide with each other. When the instruction word 414 is not written correctly in the rewritable instruction memory 409, the two instruction words do not coincide with each other. Then, a write error flag is set according to the result 417 of decision in the instruction memory control unit 408. This write error signal is not reset until all the write operations are completed. Thus, operation for writing one instruction word is completed. This operation is repeated until all the instruction words are rewritten. After all the instruction words have been rewritten, the status of the write error flag is examined. When the write error flag is set, the instruction word write operation is restarted after resetting the write error flag. When any write error flag is not set and the rewrite has been ended normally, a write end signal 418 is given to the host processor 403. Then, the host processor cancels the hold request signal 405 to cancel the temporary stop mode. Upon the cancellation of the hold request signal 405, the instruction memory control unit 408 of the signal processor 404 provides a selection signal 412 to make the switching circuit 411 select the instruction address of the PC 407, the instruction address of the PC 407 is updated, and then an instruction at an instruction address succeeding the instruction address of the last instruction word executed before the execution of instructions was stopped temporarily is executed. Thus the contents of the signal processing process can readily be changed by providing the signal processor with an internal rewritable instruction memory. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate a butterfly coprocessor within the method and apparatus of Murakami. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill would have recognized that by replacing the

host processor with a butterfly coprocessor would increase the efficiency of the system by performing high-speed butterfly operations.

As per claim 2, Murakami substantially teaches, in view of above rejections, (col. 50, lines 21-34) a digital signal processor which includes data address generator coupled to a bus.

As per claim 3, Murakami substantially teaches, in view of above rejections, (col. 49, lines 44-47) an arithmetic logic unit capable of processing the input data at least through addition, subtraction and absolute differential operation within one machine cycle.

As per claims 4-6, Murakami substantially teaches, in view of above rejections, (col. 9, lines 10-64) a conditional branch instruction is an instruction to specify executing an instruction word in a branched address specified by the instruction when the specified branch condition is met or to specify executing an instruction word in the next address. When the conditional branch instruction is decoded, a flag 69A held by the flag register 69 is read and is applied to a condition decision unit 72. The condition decision unit 72 decides whether or not the branch condition 64A specified by the instruction is met. When the branch condition 64A is met, the logical value of a branch signal 72A becomes "1", the switching circuit 71 selects the branched address 64B specified by an instruction, and then the branched address 64B is given to the PC 61. When the branch condition 64A is not met, the logical value of the branch signal 72A becomes "0", the switching circuit 71 selects the address 71A greater than the instruction address 70A by "1", and then the address 71A is given to the PC 61. Operation of the processor in a case where only information indicating whether or not A=B (A and B are input data) is met is required will be described with reference to FIG. 7. First data A.sub.0 and B.sub.0 are compared. When the data A.sub.0 is equal to the data B.sub.0, the value of a predetermined address TS(0) in the data

memory is made "1". When the data A.sub.0 is not equal to the data B.sub.0, the value of the address TS(0) is made "0". Then, data A.sub.1 and B.sub.1 are compared and the result of the comparison is written at an address TS(1). The result of comparison of data A.sub.2 and B.sub.2 is written at an address TS(2).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Murakami teaches a digital signal processor of a simple circuit configuration capable of implementing arithmetic processes and interruption processes efficiently in a reduced number of steps at a high processing speed. Applicants are invited to read/review additional pertinent prior arts of record that have been included herein.

Any inquiries concerning this communication should be directed to the examiner, Mujtaba Chaudry who may be reached at 703-305-7755. The examiner may normally be reached Mon – Thur 7:30 am to 4:30 pm and every other Fri 8:00 am to 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, Albert DeCady at 703-305-9595. The fax phone number for the organization where this application is assigned is 703-746-7239.

Any inquiry of general nature or relating to the status of this application or proceeding should be directed to the receptionist at 703-305-3900.

Mujtaba Chaudry
Art Unit 2133
April 1, 2004

ALBERT DECADY
PATENT EXAMINER